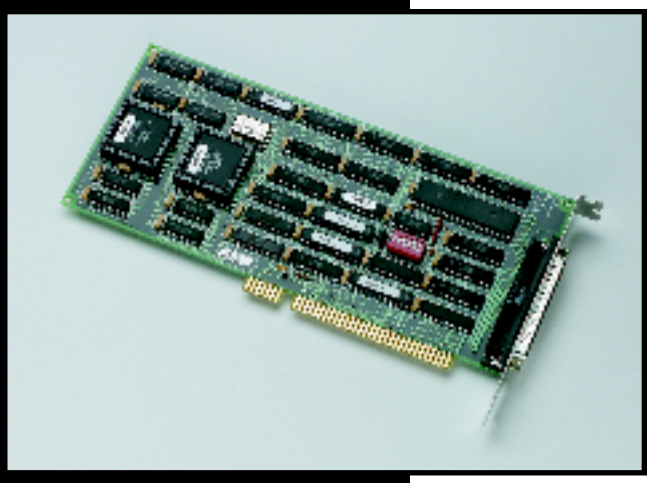
PIO-INT

24-Line Pattern Recognition Digital I/O Board



- 24 TTL/CMOS digital I/O Lines
- 16 lines with extensive interrupt capabilities
- Bit change interrupt generation
- Pattern match interrupt generation
- Flexible digital I/O based on popular 8255 PPI
- PC/XT/AT ISA and EISA bus compatible
- Uses extended interrupt levels of PC/AT
- Brings out ±12V & ±5V from PC
- DOS Software driver simplifies programming
- Programmable interrupt level selection
- Programmable interrupt delay

Ordering Information

PIO-INT Pattern Recognition Board with DOS Software

Functional Description

Keithley's PIO-INT is functionally equivalent to the popular PIO-12 but with extensive interrupt generation capabilities. It is often used to perform pattern recognition. The PA and PB ports are monitored by circuitry capable of generating interrupts either on the change of any bit in the port(s) or when a specific combination (pattern) of bits appears at the port(s). The PC port can be divided into two nibble-wide ports (PC-upper and PC-lower) and is useful as an auxiliary I/O port although it is not monitored and has no interrupt generating capabilities. The PA, PB, PC-upper and PC-lower ports may be individually configured as input or output in any combination by the 8255 control register. All ports can always be read and written to as normal 8-bit I/O ports.

There are 2 types of interrupt operations for the PA and PB ports:

1. Bit interrupts. A change of any unmasked bit either from 0 to 1 or 1 to 0 will generate an interrupt. The bit(s) that changed can be read from the Interrupt Status Register; reading this register also clears the interrupt. Only bits that are activated by the Interrupt Mask Registers (one for each port) will generate an interrupt.

2. Pattern interrupts. An interrupt is generated on a given pattern of bits in a port. Only unmasked bits (set by the mask register) can participate in a pattern match interrupt and they are compared with a stored pattern of bits in the PIO-INT's Pattern Match Registers (one for each port).

These interrupt types cover a variety of conditions under which the PIO-INT will generate an interrupt, including bit changes or pattern matches in only PA or both PA and PB ports OR'ed or AND'ed together. In addition, by masking any port, interrupts can be suppressed from that port, allowing interrupts from single or multiple bits in the other port. This gives a large variety of possible operating conditions such as:

1. No interrupts at all (disabled) — simple I/O board.
2. Interrupt on selected bit change(s) in one or both ports.
3. Interrupt on selected bit change(s) in one port and/or a pattern match in the other port.
4. Interrupt on pattern matches in either or both ports (independent 1–8 bit or full 1–16 bit matches).

On power up, all the mask and interrupt control registers are cleared, so until initialized, the PIO-INT cannot generate interrupts. In order to prevent missing interrupts while the Interrupt Service Routine (ISR) is in process, the interrupt is delayed by a two-stage digital delay. The delay time should be longer than the ISR duration. Delays are selectable independently for the PA and PB ports. The delay has a programmable clock period ranging from 100ns to 1 second. Since this is a delay and not a low pass filter, some caution is needed when transients may occur at the clock frequency, or harmonics of that frequency; if the effect of glitches combined with steady levels is to produce an interrupt condition at three successive clock pulses, that interrupt will occur.

The connector pin out is identical to the PIO-12 with the exception that no external interrupt input and enable are provided as they would be redundant (hence pins 1 and 2 of the rear connector have no connection).

Base Address, I/O Map & Interrupt Level Selection

The PIO-INT uses a contiguous block of 16 I/O addresses. The Base Address is switch-selectable and can be placed on any 16-bit I/O address boundary in the range 000H to 350H. Due to system limitations, addresses from 200H to 350H are available on the PC and PC/XT, and addresses from 100H to 350H are available on the PC/AT. Allowing for other plug-in boards, there will still be a wide choice of unused I/O address options available in any computer. On a PC/AT or EISA/ISA bus computer, the PIO-INT can be programmed to operate on bus interrupt levels 2, 3, 4, 5, 7, 10, 11, 12, 14, or 15. When used in a PC/XT slot, only levels 2, 3, 4, 5, or 7 may be used due to the XT bus structure.

ACCESSORIES AVAILABLE

C1800	PIO-INT to STA-U or STP-37 Cable
STA-U	Universal Screw Terminal Accessory
STC-37	Direct Screw Terminal Connector
STP-37	Screw Terminal Panel
MS-PIO-INT	Additional Hardware Manual and DOS Software

Extensive interrupt generation capabilities

PCI/ISA/PCMCIA

1.888.KEITHLEY (U.S. only)

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A GREATER MEASURE OF CONFIDENCE

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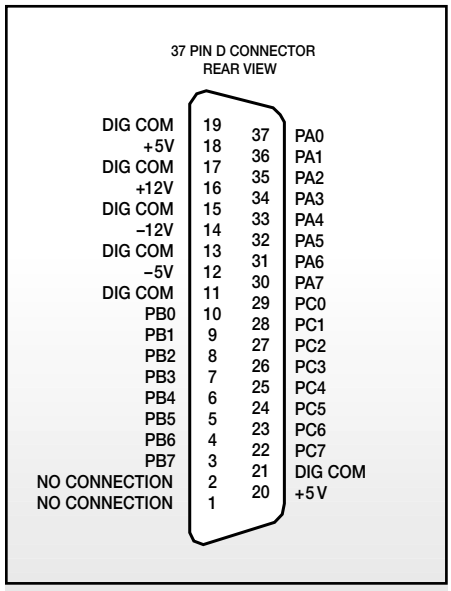
Programming

The PIO-INT is supported by a comprehensive set of DOS drivers and programming tools. Standard software provided with the PIO-INT includes the following:

- Mode Call Drivers compatible with BASICA, and QuickBASIC, Pascal, Turbo Pascal, most versions of C, and FORTRAN.
- PIO-INT installation and configuration program.
- A variety of example programs which show how to write PIO-INT programs in all supported languages.
- Complete diagnostic and test routine.

The Mode Call Drivers are a collection of functions that are accessed from your program through a single line subroutine CALL statement. The various modes of the Call routine select the function to perform, format and error check the data and perform frequently used sequences of instructions.

Connector Pin Assignment



APPLICATIONS

- **General purpose & interrupt driven digital I/O**
- **Contactor switch change monitoring**
- **Bit pattern matching or comparison**
- **Process activation on defined bit states or changes**

Specifications

LOGIC INPUTS AND OUTPUTS

	Min	Max
INPUT LOGIC LOW VOLTAGE:	–0.5V	+0.8V
INPUT LOGIC HIGH VOLTAGE:	+2.0V	+5.0V
INPUT CURRENT LOGIC LOW, PA & PB PORTS:	—	0.4mA
PC PORT:	–10µA	+10µA
INPUT CURRENT LOGIC HIGH, PA & PB PORTS:	—	+40µA
PC PORT:	–10µA	+10µA
OUTPUT LOW VOLTAGE, I_{SINK} = 1.4mA ALL PORTS:	—	+0.45V
OUTPUT HIGH VOLTAGE, I_{SOURCE} = 200µA ALL PORTS:	+2.4V	+5.5V

INTERRUPT LEVELS SUPPORTED

PC & PC/XT (5 LEVELS): 2, 3, 4, 5, 7.

PC/AT (10 LEVELS): 2, 3, 4, 5, 7, 10, 11, 12, 14, 15.

PROGRAMMABLE INTERRUPT DELAY

CLOCK PERIOD: 100ns, 1µs, 10µs, 100µs, 1ms, 10ms, 100ms, 1s. For reliable interrupt generation, input pulse width must be more than 2 times the selected clock period.

ENVIRONMENTAL

OPERATING TEMPERATURE RANGE: 0 to +50°C.

STORAGE TEMPERATURE RANGE: –40 to +100°C.

HUMIDITY: 0 to 90% non-condensing.

DIMENSIONS: 9.0in L × 4.25in H × 0.75in D (22.9cm × 10.8cm × 1.9cm).

Configuration Guide